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Low Power Standard Logic Gate Cells Design and its Power & Delay Analysis

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Abstract- This paper describes the design of a 45nm CMOS technology standard logic library cell for highly energy-efficient applications of embedded processors.Design of Inverter, NOR and NAND circuits is present in this paper to improve the speed and power. The comparative analysis of different performance parameters for CMOS logic gates is presented. Average power, Static Power and Delay are the parameters evaluated using Cadence tool. For a full-chip implementation of low-power systems operating at ultra-low voltage is feasible. The power and delay is extracted for logic cells at supply voltages 0.8 V, 1.0 V & 1.2 V at different frequencies.
Keywords: - Low power Design, Power-delay product, CMOS Technology.

I.INTRODUCTION

In IC design technology where numbers of logic gates are integrated, constant and continuous works is being carried out by different experts to reduce the power dissipation. It is still a big challenge for researchers to design a reliable circuit with very low power dissipation [1]. There are different approaches to minimize the power dissipation base on architecture, circuit level, layout, and process technology. Among all these techniques, at the circuit design level considerable amount of power savings [2] can be achieve by means of proper choice of a logic style for implementing combinational circuits. This is because all the important parameters governing power dissipation, switching capacitance, transition activity, and short-circuit currents[3] are strongly influenced by the chosen logic circuit. Another approach to reduce power dissipation [4] is by using stack technique where each of the NMOS and PMOS in the logic gate is split into two transistors. Sub threshold [5] circuit design operation technique also reduces power dissipation in CMOS where circuits should be operated in near-threshold region [6]. Another effective way is by reducing the supply voltage as CMOS total power dissipation depends upon two power i.e. dynamic power and static power[7]. As these both power depends upon VDD if supply voltage [8] is reduced the total power can be minimize.

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II. GENERAL REVIEW OF TOTAL POWER CONSUMPTION IN CMOS.

The basic equation governing the total power in CMOS circuit is given by

$$P_{Total} = P_{Dynamic} + P_{Static}$$

$$P_{Total} = ½\ C_L V_{DD}^2 \alpha f + I_{Sc} V_{DD} + I_{Static} V_{DD} \quad (1)$$

Where C_L is the load capacitance, f is the frequency of operation, α is the activity factor, I_{Sc} is the short circuit current [9]. The equation (1) implies that both the dynamic and static power depends upon the supply voltage VDD [10] at large. The dynamic power consumption is mainly due to the charging and dis-charging of the capacitance and short circuit current. A short circuit current flows when the pull up and pull down networks in a CMOS circuit are simultaneously on and a direct path exists between the supply line and ground. Dynamic power [11] is directly proportional to the square of the supply voltage. Therefore, dynamic power reduces in a quadratic manner when the supply voltage is reduced. Leakage power is dependent on the leakage current [12] flowing in the CMOS circuit. If the supply voltage VDD is reduced the total power dissipation in the CMOS circuit [13] can be decrease tremendously. This work is carried out at supply voltage of 0.8V, 1.0V 1.2V with 45nm CMOS technology by scaling the size[14] of MOS transistor to its minimum optimum level so that the basic gate operation is not affected.

III.CIRCUIT IMPLEMENTATION

The Design of logic gates includes universal logic gates(NAND gate, NOR gate) and Inverter. Schematic & Layouts are developed for logic gates and Simulation is carried out with a supply voltageof 0.8V, 1.0V & 1.2V at different frequencies (100MHz, 200MHz, 250MHz, 400MHz 500MHz). Average power and delay [15] is measured at different supply voltages and frequencies. A stream of bits is used as input bits. Each of the bits with magnitude 0.8V,1.0V &1.2V corresponds to logic 1 and the ground state corresponds to logic 0. NAND & NOR Gates are simulated with two input terminal A and B with output terminal Q.

3.1 INVERTER (NOT GATE)

NOT gate is also known as inverter which performs bitwise operation of inverted input as output. When all the input are high (logic ’1’) then the output is low (logic ‘0’) as well as the other operation. The truth table for NOT gate is given below. In the same way the 32-bit NOT gate performs operation on individual bit of 32-bit input A.

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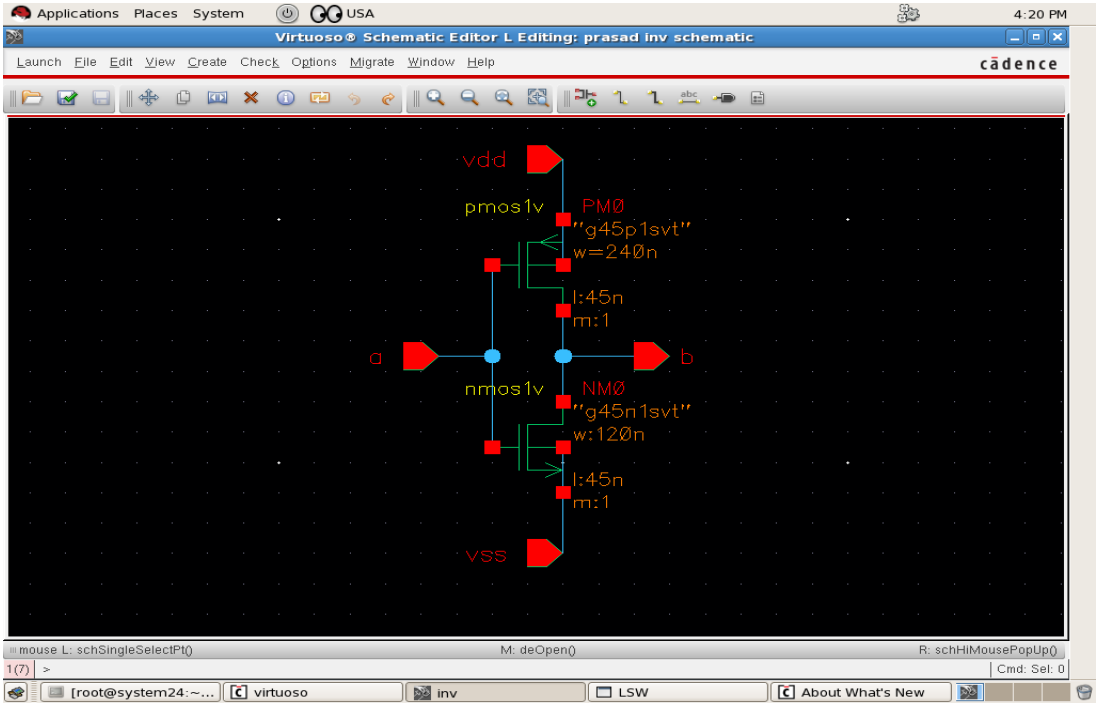

Fig: 1 Schematic circuit of Inverter

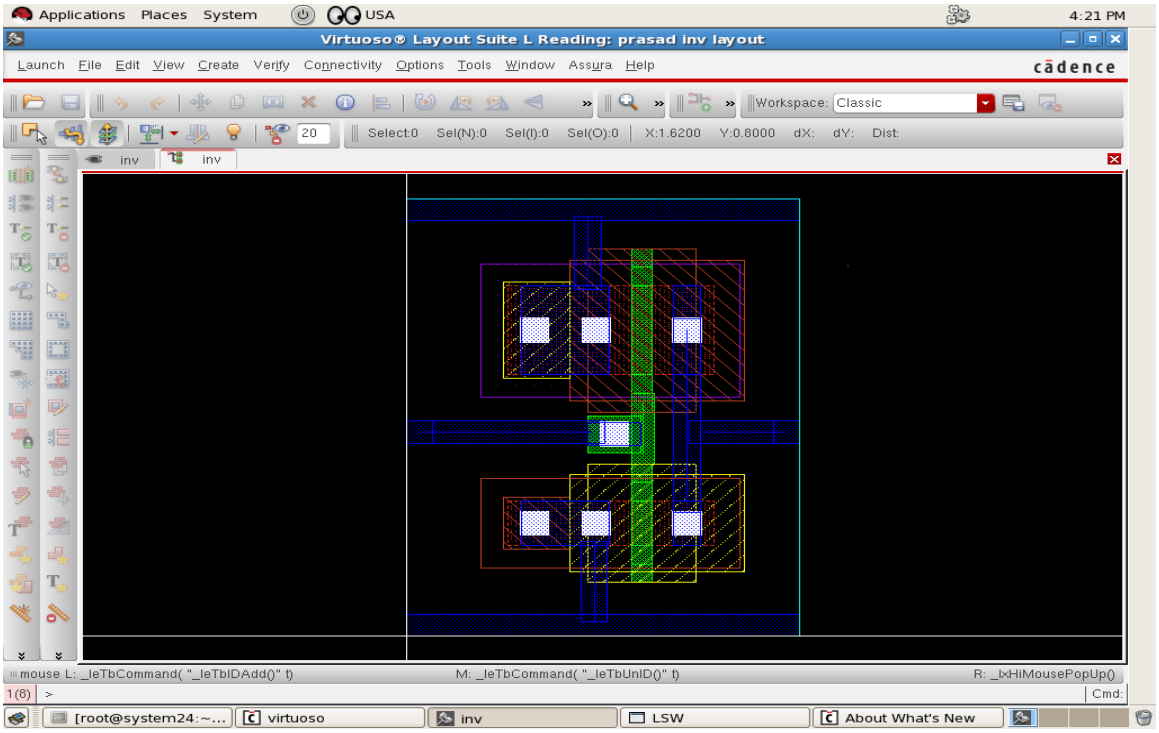

Fig: 2: Layout circuit of Inverter

Fig :1shows schematic circuit&Fig:2 shows layout diagrams of Inverter

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3.1.1 Power, Delay and PDP Results and Analysis of Inverter:-

Schematic Average Power(nW)					
Supply Voltage(V)	Frequency(MHz)				
	100	200	250	400	500
0.8	24.33	48.61	60.79	97.26	121.6
1.0	35.21	70.41	88.00	140.8	176.2
1.2	47.44	94.86	118.6	189.7	237.1

Table 1: Schematic power consumption of Inverter

Layout Average Power(nW)					
Supply Voltage(V)	Frequency(MHz)				
	100	200	250	400	500
0.8	34.37	68.71	85.90	137.0	171.2
1.0	50.91	101.8	127.3	203.6	254.5
1.2	69.41	138.8	173.5	277.5	346.9

Table 2: Layout power consumption of Inverter

Static Power(pW)		
Supply Voltage(V)	Schematic Power	Layout Power
0.8	2.37076	2.37069
1.0	3.53591	3.53581
1.2	4.92533	4.92518

Table 3: Static power consumption of Inverter

Table 1 shows average power of schematic circuit at different supply voltage and different operating frequencies. Table 2 shows average power of layout at different supply voltage and different operating frequencies.Table 3 shows static power of Inverter at different supply voltages.

	Schematic Delay(pS)		Layout Delay(pS)	
Supply Voltage(V)	Minimum	Maximum	Minimum	Maximum
0.8	8.720	11.40	11.08	14.893
1.0	7.034	8.608	5.684	6.870
1.2	4.406	5.292	5.487	6.525

Table 4: Delay comparison of Inverter

Schematic Power Delay Product(aW-S)					
Supply Voltage(V)	Frequency(MHz)				
	100	200	250	400	500
0.8	0.277	0.554	0.693	1.109	1.386
1.0	0.303	0.606	0.756	1.212	1.517
1.2	0.251	0.501	0.918	1.004	1.255

Table 5: Schematic PDP of Inverter

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Layout Power Delay Product(aW-S)					
Supply Voltage(V)	Frequency(MHz)				
	100	200	250	400	500
0.8	0.512	1.023	1.279	2.040	2.550
1.0	0.350	0.699	0.875	1.399	1.748
1.2	0.453	0.906	1.132	1.811	2.264

Table 6: Layout PDP of Inverter

Table 4 shows delay for Schematic & Layout design, Table 5 shows Power-Delay product of Schematic design and Table 6 shows Power-Delay product of Layout design of Inverter.

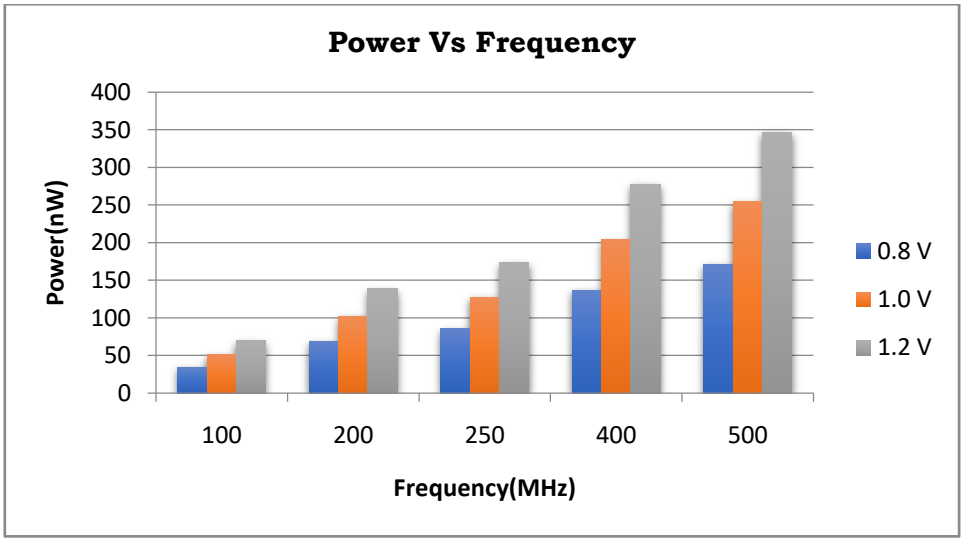

Fig: 3Power comparison of Inverter at 0.8 V,1 V & 1.2 V supply voltage

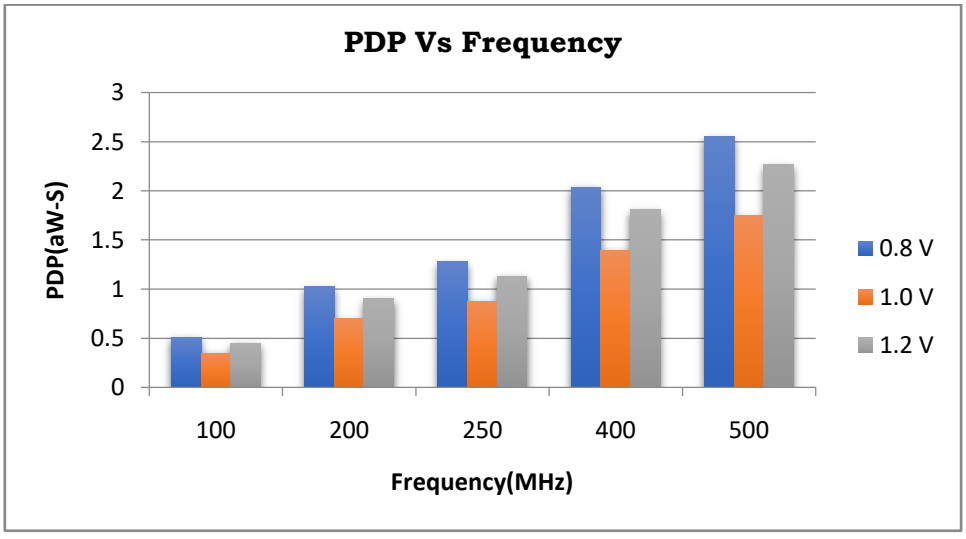

Fig: 4 PDP comparison of Inverter at 0.8 V, 1V & 1.2 V supply voltage

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Fig 3 shows comparison of Layout power at different frequencies and supply voltages and Fig 4 comparison PDP at different frequencies and supply voltages of Inverter.

3.2 NAND gate

NAND gate is one of the universal gates which performs bitwise operation on two or more number of inputs. When all the inputs are high (logic '1') then the output is low (logic '0').In the remaining cases, the output is high(logic '1'). The truth table for two input NAND gate is given below. In the same way the 32-bit NAND gate performs operations on individual bits of two inputs A and B.

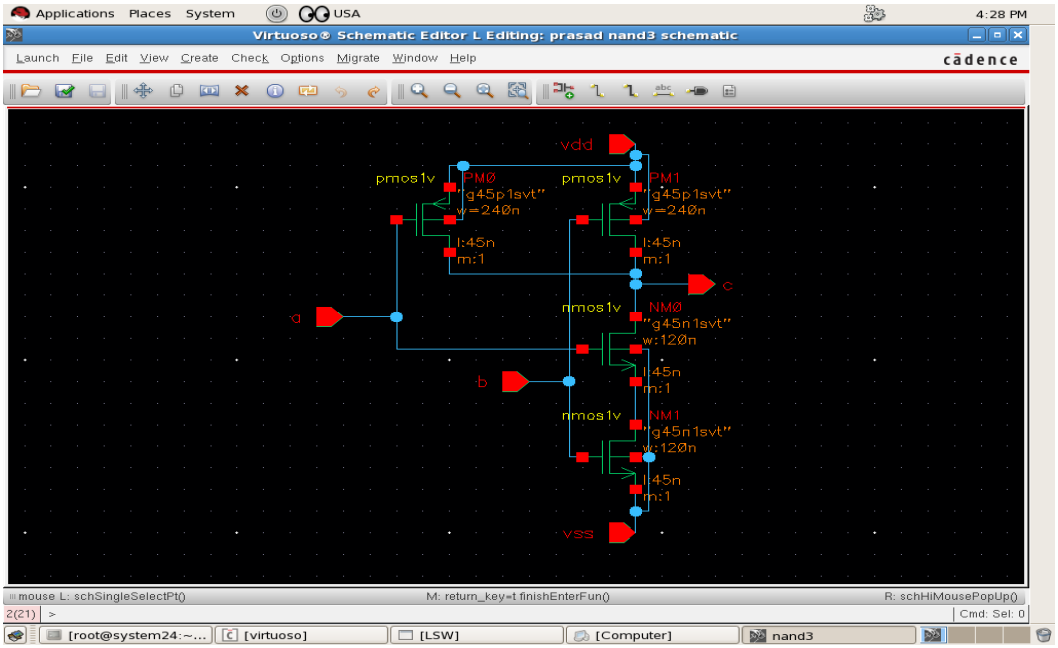

Fig: 5 Schematic circuit of NAND gate

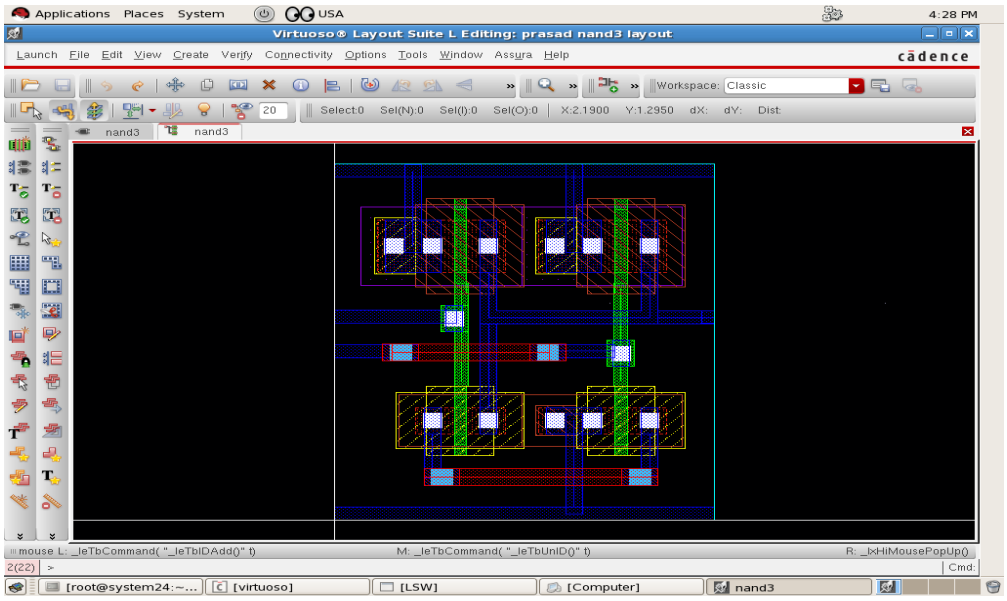

Fig: 6 Layout circuit of NAND gate

Fig :5shows schematic circuit& Fig:6shows layout diagrams of NAND Gate.

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3.2.1 Power, Delay and PDP Results and Analysis of NAND gate:-

Schematic Average Power(nW)					
Supply Voltage(V)	Frequency(MHz)				
	100	200	250	400	500
0.8	22.96	45.39	56.52	89.73	111.7
1.0	35.33	69.98	87.2	138.6	172.6
1.2	49.42	98.06	122.2	194.5	242.4

Table 7: Schematic power consumption of NAND gate

Layout Average Power(nW)					
Supply Voltage(V)	Frequency(MHz)				
	100	200	250	400	500
0.8	45.69	90.54	112.8	179.5	223.6
1.0	70.77	140.4	175.0	278.5	347.2
1.2	99.36	197.2	245.8	391.4	488.1

Table 8: Layout power consumption of NAND gate

Static Power(pW)		
Supply Voltage(V)	Schematic Power	Layout Power
0.8	4.74151	4.74116
1.0	7.07182	7.07127
1.2	9.85067	9.84988

Table 9: Static power consumption of NAND gate

Table 7 shows average power of schematic circuit at different supply voltage and different operating frequencies. Table 8 shows average power of layout at different supply voltage and different operating frequencies.Table 9 shows static power of NAND Gate at different supply voltages.

	Schematic Delay(pS)		Layout Delay(pS)	
Supply Voltage(V)	Minimum	Maximum	Minimum	Maximum
0.8	7.96	35.4	12.22	65.2
1.0	5.37	17.2	7.76	30.7
1.2	4.14	11.8	6.05	20.8

Table 10: Delay comparison of NAND gate

Schematic Power Delay Product(aW-S)					
Supply Voltage(V)	Frequency(MHz)				
	100	200	250	400	500
0.8	0.813	1.607	2.001	3.176	3.954
1.0	0.608	1.204	1.500	2.384	2.969
1.2	0.583	1.157	1.442	2.295	2.860

Table 11: Schematic PDP of NAND gate

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Layout Power Delay Product(aW-S)					
Supply Voltage(V)	Frequency(MHz)				
	100	200	250	400	500
0.8	2.979	5.903	7.355	11.703	14.579
1.0	2.173	4.310	5.373	8.550	10.659
1.2	2.067	4.102	5.113	8.141	10.153

Table 12: Layout PDP of NAND gate

Table 10 shows a delay comparison of NAND gate. Table 11 represent the Schematic PDP of NAND gate. Table 12 shows a layout PDP of NAND gate.

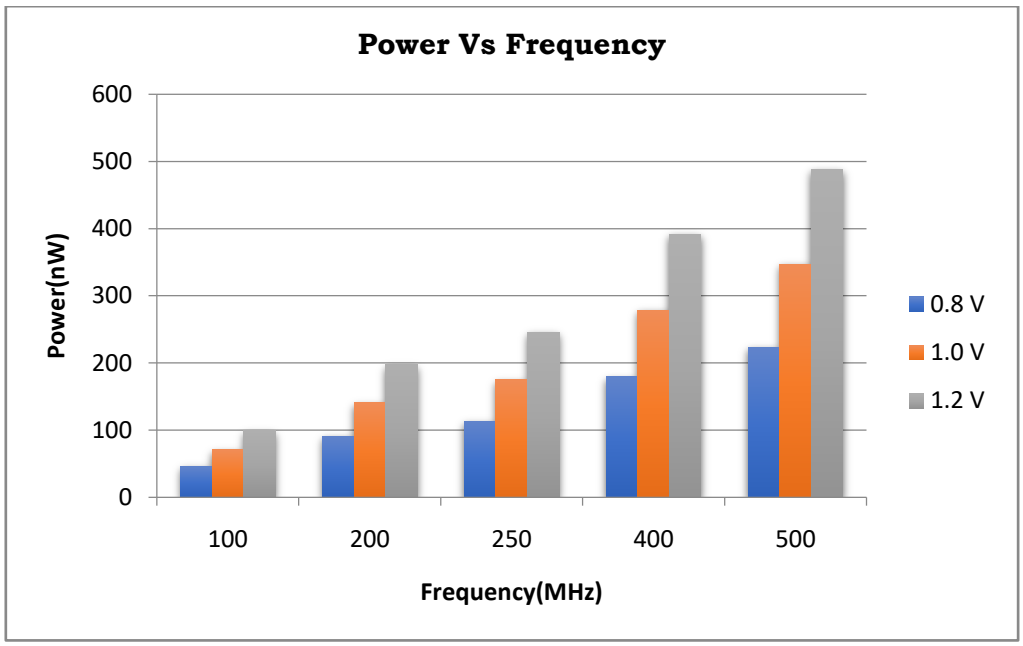

Fig: 7 Power comparison of NAND gate at 0.8 V, 1V, 1.2 V supply voltage

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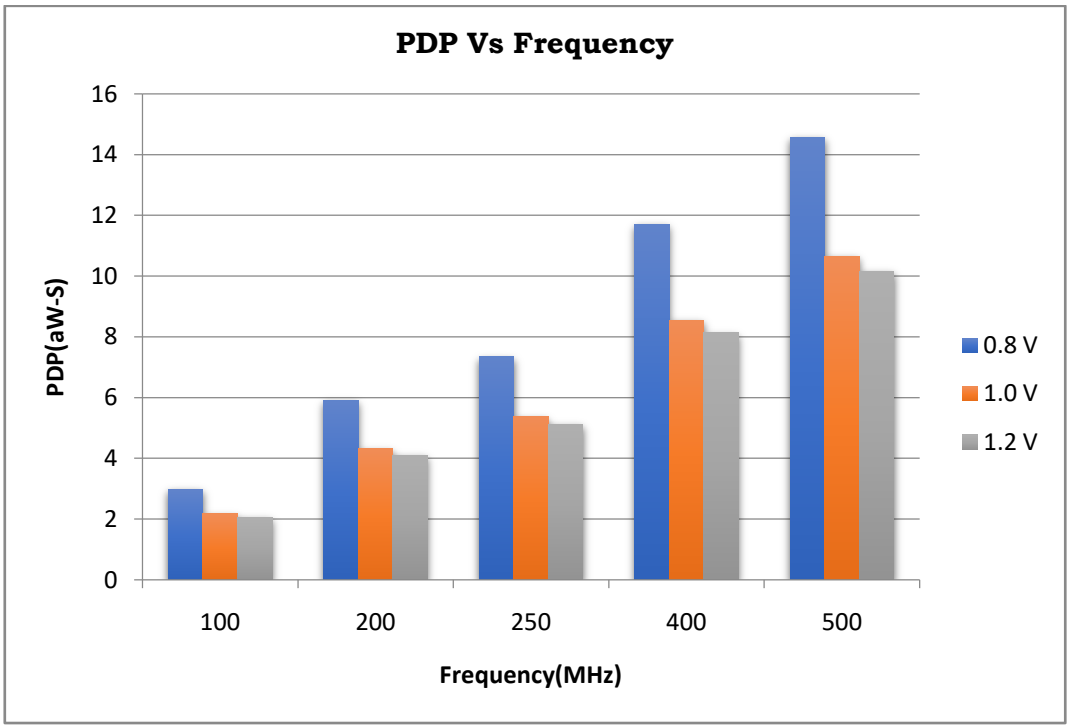

Fig: 8 PDP comparison of NAND gate at 0.8 V, 1V, 1.2 V supply voltage

Fig 7 shows comparison of Layout power at different frequencies and supply voltages and Fig 8 comparison PDP at different frequencies and supply voltages of NAND Gate.

4.3 NOR GATE

NOR gate is one of the universal gates performs bitwise operation on two or more number of inputs. When all the inputs are low (logic ’0’) then the output is high (logic ‘1’).In the remaining cases, the output is low(logic ‘0’). The truth table for two input NOR gate is given below. In the same way the 32-bit NOR gate performs operations on individual bits of two inputs A and B.

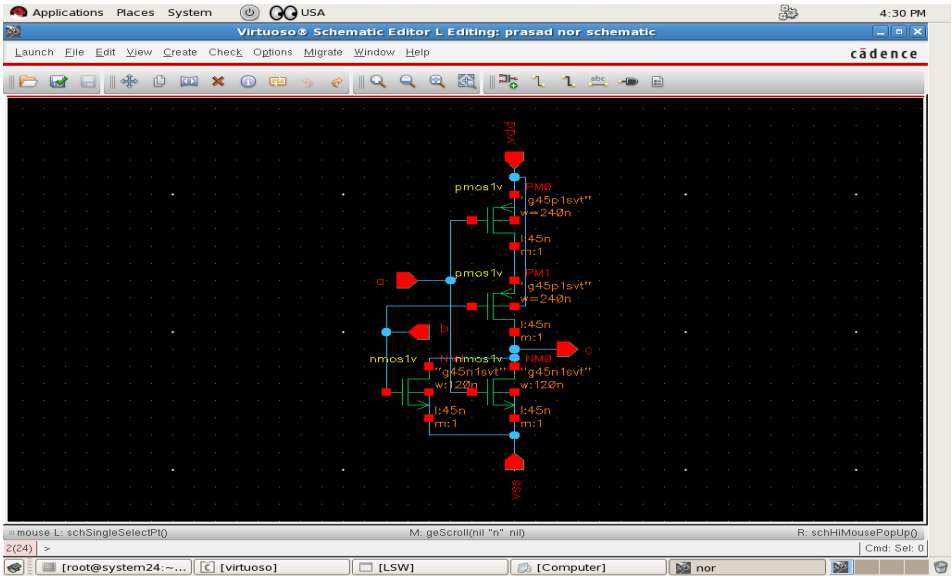

Fig: 9 Schematic circuit of NOR gate

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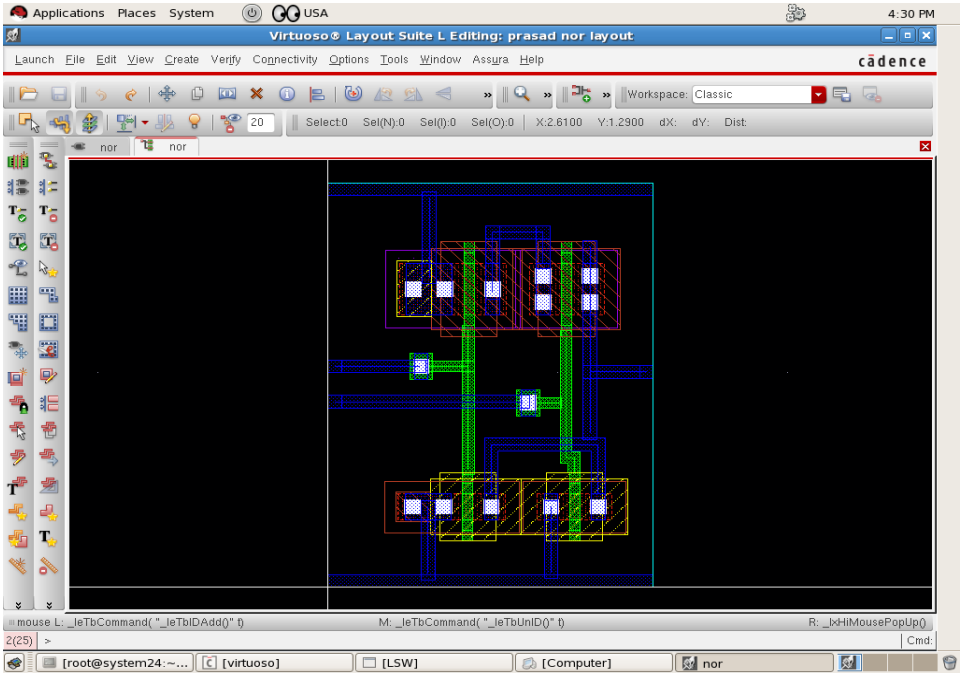

Fig: 10Layout circuit of NOR gate

Fig :9shows schematic circuit& Fig:10 showslayout diagrams of NOR Gate.

4.3.1 Power, Delay and PDP Results and Analysis of NOR gate:-

Schematic Average Power(nW)					
Supply Voltage(V)	Frequency(MHz)				
	100	200	250	400	500
0.8	25.34	50.66	63.21	100.6	125.3
1.0	43.33	86.94	108.6	173.4	216.2
1.2	67.85	136.4	170.4	272.3	340.0

Table 13: Schematic power consumption of NOR gate

Layout Average Power(nW)					
Supply Voltage(V)	Frequency(MHz)				
	100	200	250	400	500
0.8	40.38	80.58	100.6	160.1	199.5
1.0	66.42	133.0	166.1	265.1	330.8
1.2	100.4	201.4	251.8	402.2	502.1

Table 14: Layout power consumption of NOR gate

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Static Power(pW)		
Supply Voltage(V)	Schematic Power	Layout Power
0.8	1.27090	1.27097
1.0	1.90438	1.90450
1.2	2.67041	2.67059

Table 15: Static power consumption of NOR gate

Table 13 shows average power of schematic circuit at different supply voltage and different operating frequencies. Table 14 shows average power of layout at different supply voltage and different operating frequencies.Table 15 shows static power of NOR Gate at different supply voltages.

	Schematic Delay(pS)		Layout Delay(pS)	
Supply Voltage(V)	Minimum	Maximum	Minimum	Maximum
0.8	13.25	27.7	21.54	42.4
1.0	7.88	14.8	12.1	22.2
1.2	6.02	10.64	9.05	15.7

Table 16: Delay comparison of NOR gate

Schematic Power Delay Product(aW-S)					
Supply Voltage(V)	Frequency(MHz)				
	100	200	250	400	500
0.8	0.702	1.403	1.751	2.787	3.471
1.0	0.641	1.287	1.607	2.566	3.200
1.2	0.722	1.451	1.813	2.897	3.618

Table 17: Schematic PDP of NOR gate

Layout Power Delay Product(aW-S)					
Supply Voltage(V)	Frequency(MHz)				
	100	200	250	400	500
0.8	1.712	3.417	4.265	6.788	8.459
1.0	1.475	2.953	3.687	5.885	7.344
1.2	1.576	3.162	3.953	6.315	7.883

Table 18: Layout PDP of NOR gate

Table 16 shows the delay comparison of NOR gate. Table 17 represent the schematic PDP of NOR gate. Table 18 shows a layout PDP of NOR gate.

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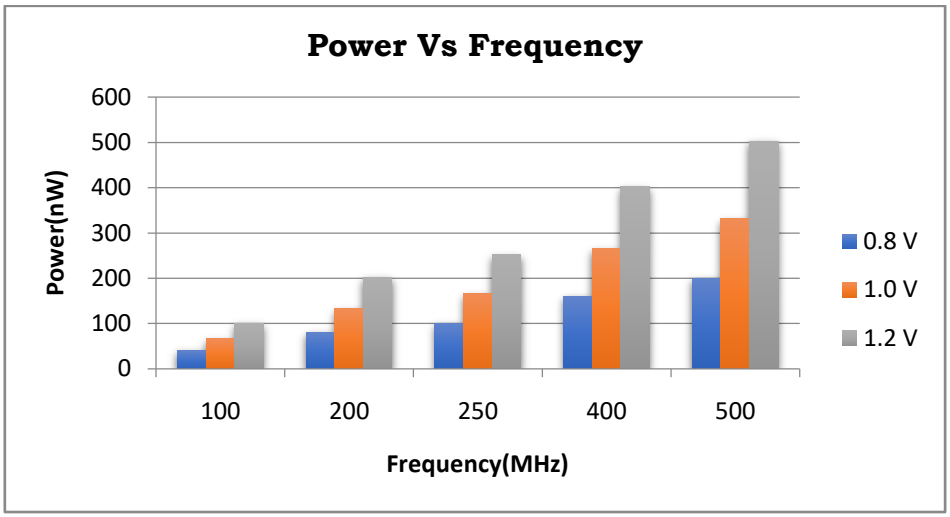

Fig: 11 Power comparison of NOR gate at 0.8 V, 1V, 1.2 V supply voltage

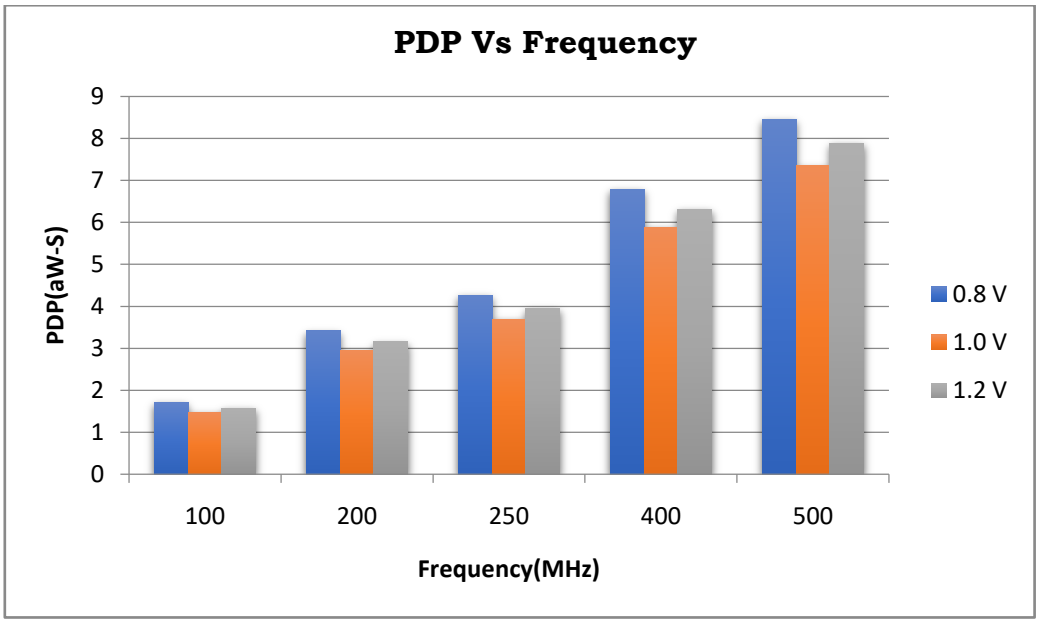

Fig: 12 PDP comparison of NOR gate at 0.8 V, 1V, 1.2 V supply voltage

Fig 11 shows comparison of Layout power at different frequencies and supply voltages and Fig 12 comparison PDP at different frequencies and supply voltages of NOR Gate.

IV.CONCLUSION:

In order to perform basic arithmetic operations Inverter, NAND & NOR gates are designedusing 45nm CMOS Technology which consumes very less power. The delay comparison is also done & Power Delay Product (PDP) is calculated.Our experimental results show that the average power of NANDis reduced by40%when supply voltage is changing from 1.2V to 1.0V at 500 MHz. Average power is reduced to 55% when supply voltage changing from 1.0V to 0.8 V at 500 MHz.The average power of NORis reduced by 51% when supply voltage is changing from 1.2V to 1.0V at 500 MHz. Average power is reduced to 65% when supply voltage changing from 1.0V to 0.8 V at 500 MHz. By reducing

supply voltage, power reduction is achieved effectively for logic gatedesign.

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